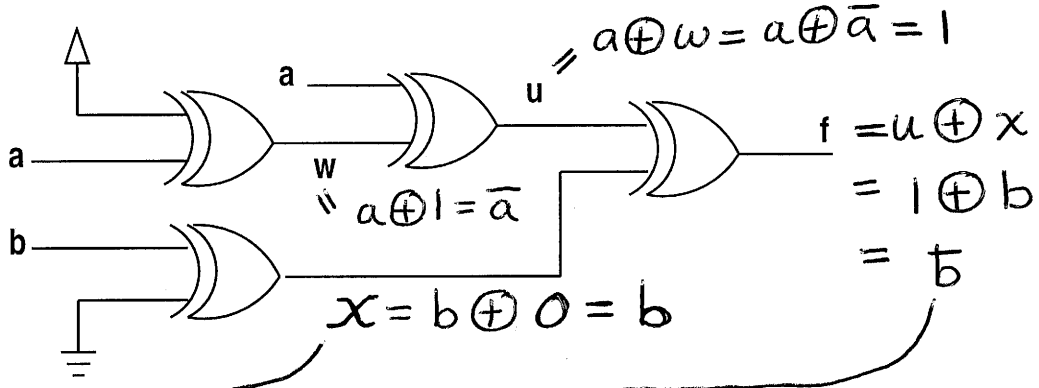
**EECS 281: Homework #2** **Due: Tuesday, January 25, 2005**

Name: Prof. Wolff Email: _____

1. Given the following schematic (study Wakerly p410-p413)




(a) Give the Truth Table for $a$, $b$, $w$, $u$ and $f$.

| a | b | x | w | u | f | $\bar{b}$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |

(b) Give the structural boolean expression of $w$, $u$ and $f$:

$w =$ $a \oplus 1$

$u =$ $a \oplus w = a \oplus (a \oplus 1)$ #1 or #2

$f(a,b) =$ $u \oplus x = (a \oplus (a \oplus 1)) \oplus (b \oplus 0)$

(c) Re-write as a structural VHDL expression:

$f <=$ (a XOR (a XOR 1)) XOR (b XOR 0)

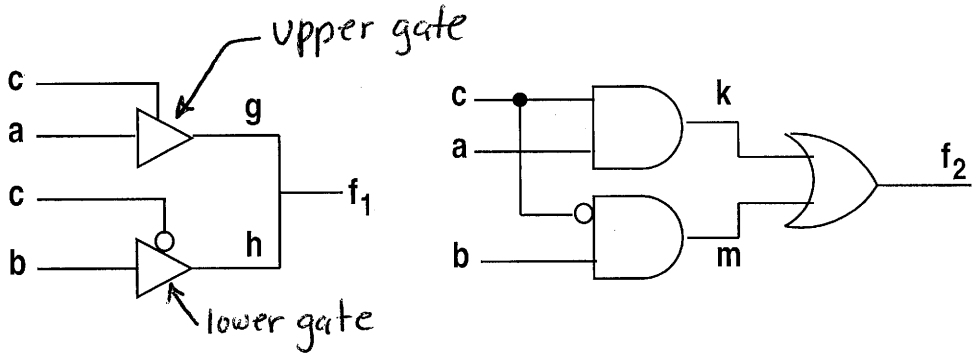
(d) Re-write as a structural C++/JAVA expression using bitwise operators:

$f =$ (a ^ (a ^ 1)) ^ (b ^ 0)

(e) Looking at the Truth Table, what is the simplest Boolean expression

$f(a,b) =$ $\bar{b}$

2. Given the following logic circuits with inputs a, b and c (study Wakerly page 126, 385-387)

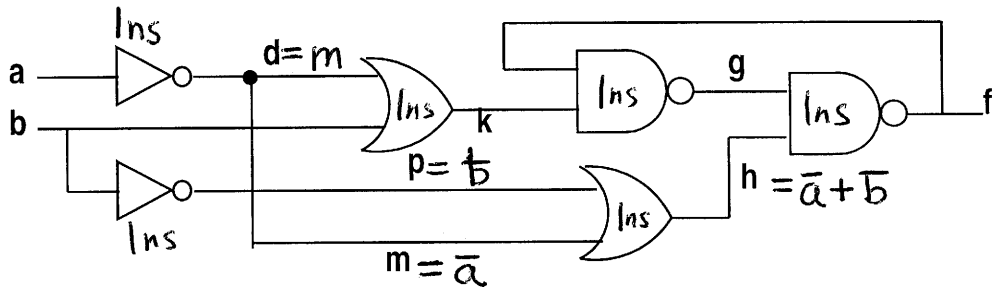


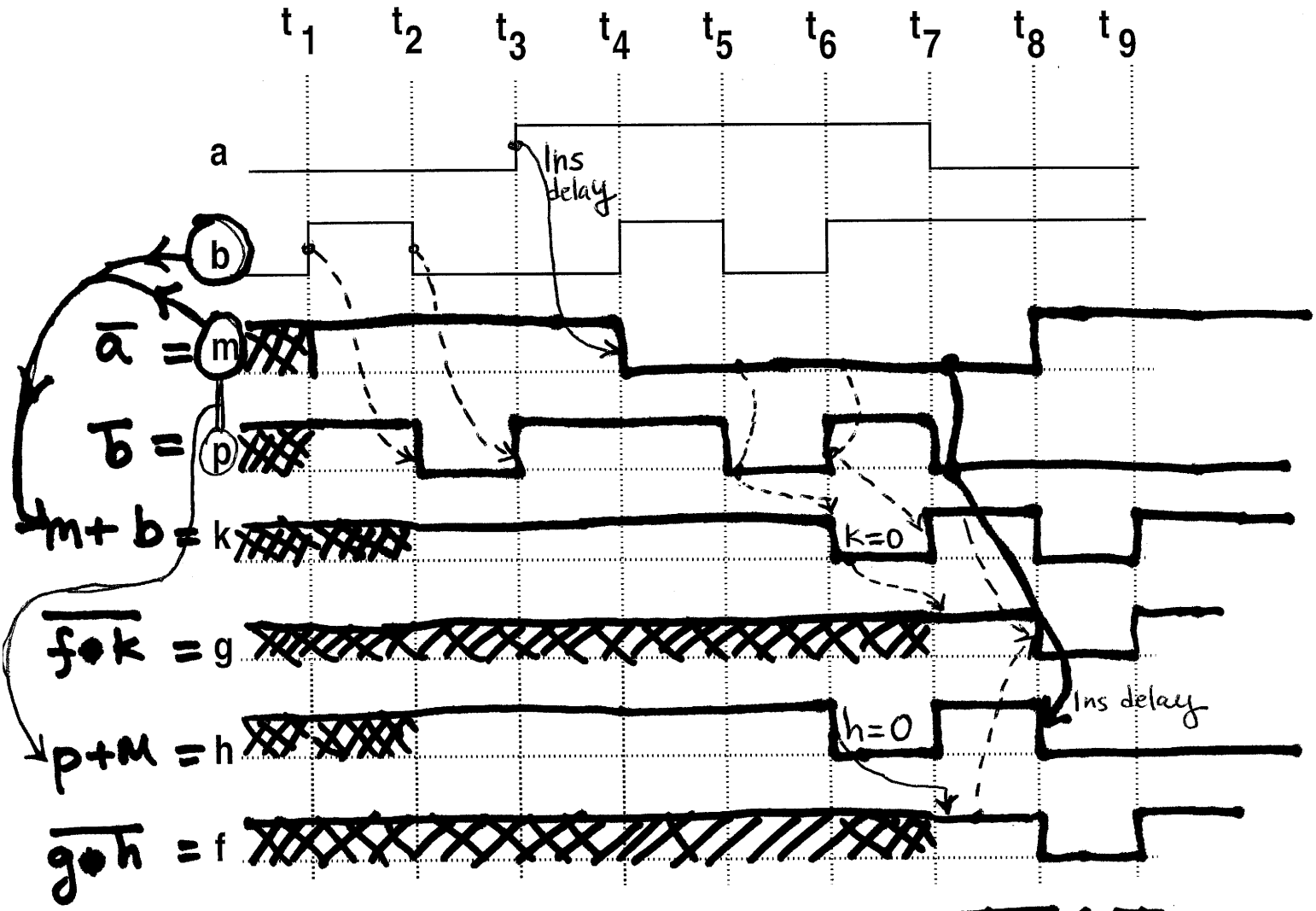

(a) Give the truth table for $f_1$ and $f_2$ showing $g$, $h$, $k$ and $m$. Calculate the outputs $g$ and $h$ as if they were not connected together in $f_1$. Calculate $f_1$ as with $g$ and $h$ connected as a single wire.

| c | a | b | upper gate | lower gate | g | h | $f_1$ | $K = c \cdot a$ | $m = \bar{c} \cdot b$ | $f_2 = K + m$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | dis | en | Z | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | | | | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | dis | en | Z | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | | | | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | en | disabled | 0 | Z | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | | | 0 | Z | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | en | disabled | 1 | Z | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | | | 1 | Z | 1 | 1 | 0 | 1 |

(b) Are $f_1$ and $f_2$ functionally (behaviourally) the same? Yes or No.
Are $f_1$ and $f_2$ structurally the same? Yes or No.

3. Give the timing diagram showing trigger lines for the following logic circuit (study Wakerly page 535) Every gate 1 nanosecond delay




hint: $g = \overline{f \bullet k}$ look for when $k = 0$ then $\overline{f \cdot 0} = \overline{0} = 1$

NAND = $\overline{0 \cdot 0} = \overline{0} = 1$

$\overline{1 \cdot 0} = \overline{0} = 0$

$h = 0$ then don't care about $g$

$f = \overline{g \cdot h}$ look for

4. Do the following Wakerly problems (Due on Thursday)

(a) 3.14, page 185

(a) 3.59, page 188

(a) 3.60, page 188

(a) 3.61, page 188

(a) 3.62, page 188

## Review

NMOS, n-channel, $V_g - V_s > V_t$ is ON

PMOS, p-channel, $V_g - V_s < V_t$ is ON

if $V_t = 0$ then

$V_g > V_s$ or $V_{gs} > 0$ is ON for NMOS

$V_g < V_s$ or $V_{gs} < 0$ is ON for PMOS

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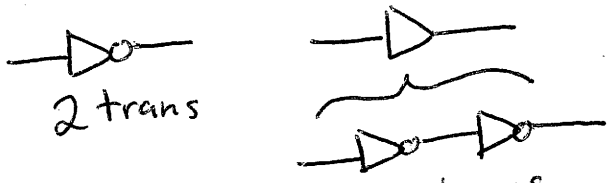
3.14




} Inverter has fewer for CMOS technology

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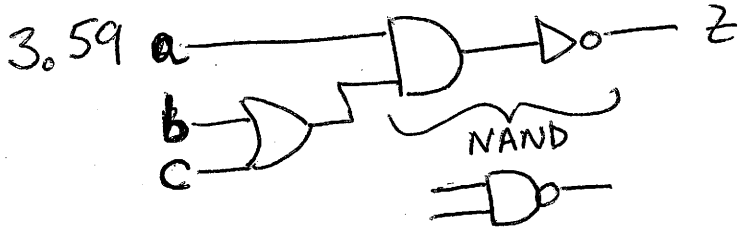
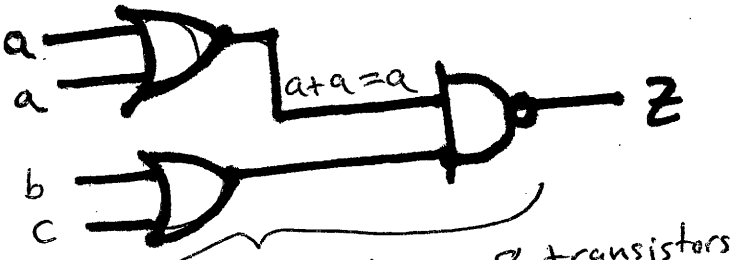
3.59



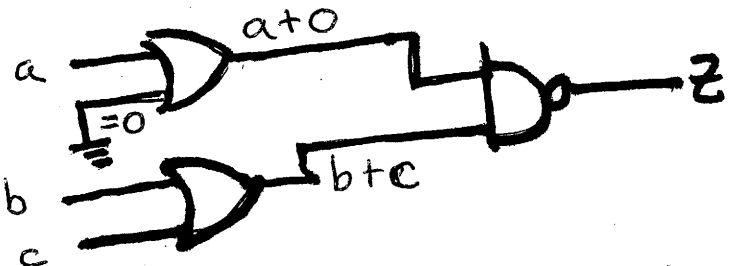




attempt #1 = 8 transistors

In Figure 3-22, OAI page 95

let A = a
B = 0 = ground (Q4, Q3)
C = b
D = c

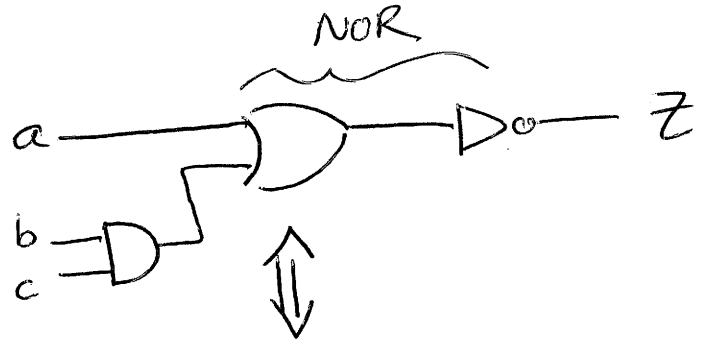
then replace Q4 with a wire from Drain to Source
remove Q3 the NMOS

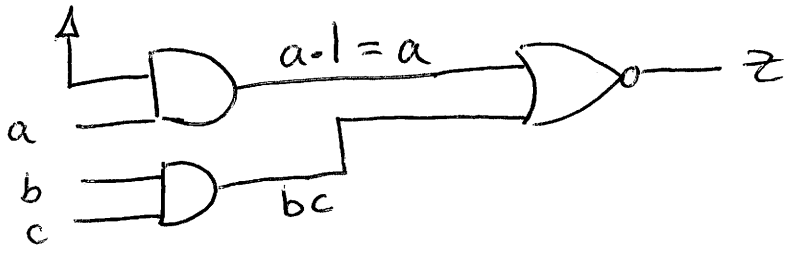



attempt #2 = 6 transistors

because if we ground (=0) the input the we can replace the NMOS with ope and the PMOS with a wire

3.60




AOI-gate

In Figure 3-20, AOI-gate, page 94

let A = 1
B = a
C = b
D = c

then
A = 1 means the NMOS at Q1 is always ON and the PMOS at Q2 is always OFF

So replace Q1 with a wire from drain to source remove Q2 the PMOS

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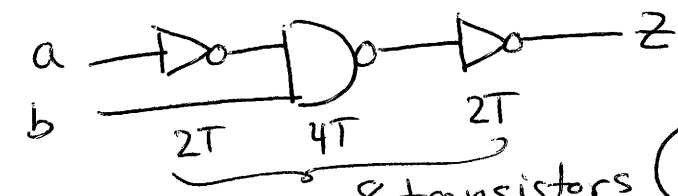
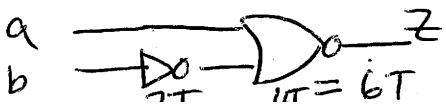
3.61

| | a | b | z |
|---|---|---|---|
| $\bar{A}\bar{B}$ | 0 | 0 | 0 |
| $\bar{A}B$ | 0 | 1 | $1 = \bar{A}B$ |
| $A\bar{B}$ | 1 | 0 | 0 |
| $AB$ | 1 | 1 | 0 |


8 transistors

cancel ⇓ Demorgan




⇐

3.62

| | a | b | z | $\bar{z}$ |
|---|---|---|---|---|
| $\bar{a}\bar{b}$ | 0 | 0 | 1 | 0 |
| $\bar{a}b$ | 0 | 1 | 1 | 0 |
| $a\bar{b}$ | 1 | 0 | 0 | $1 = a\bar{b} = \bar{z}$ |
| $ab$ | 1 | 1 | 1 | 0 |

$\bar{z} = a\bar{b}$

$z = \overline{a\bar{b}}$ ⟶