EECS 281: Homework #3 Due: Tuesday, February 1, 2005

Name: _____ Email: _____

(1a) Please download and install

PC windows: http://www.winspice.com

MacOS: http://newton.ex.ac.uk/teaching/CDHW/MacSpice/

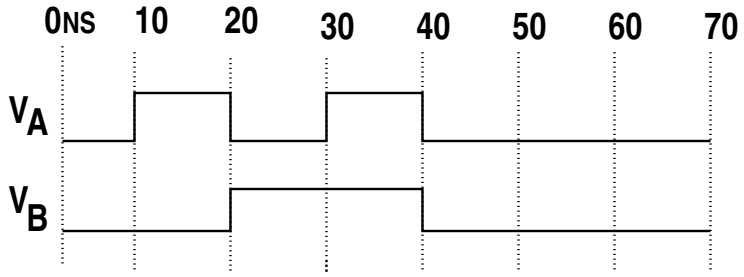
EECS dept: already installed on the machines in Olin 4th floor.

(1b) Please read the SPICE tutorial on

http://bear.ces.cwru.edu/eecs_cad/tut_spice3_invertor.html

http://www.allaboutcircuits.com/vol_5/chpt_7/3.html

(1c) Write the SPICE piece-wise linear (PWL) waveform to be used in parts 1d and 1e for the following timing diagram for inputs, A and B. Use a rise and fall time of 0.1 nanoseconds and a logic level TRUE as 5 volts and FALSE as 0 volts.



(1d) Implement the CMOS AND-gate of Figure 3-19 (see Wakerly page 93) in SPICE using the waveform input of part 1c. Assign input node A as wire "1", B as wire "2", output node Z as wire "3", V_{dd} as wire "4" and ground (i.e. GND) is always wire "0".

Use a `".TRAN 0.1N 70N"` for your waveform simulation time. Plot the voltages on wires 1, 2 and 3 as seperate plots (i.e. `"plot v(1)"`, `"plot v(2)"`, `"plot v(3)"`) and combined into a single plot (e.g. `"plot v(1),v(2),v(3)"`). Compare the plots with your expected output for an AND-gate. Use a print screen to show all plots. Hand in the netlist of the SPICE circuit (i.e. source code, or .cir file).

(1e) Re-write part 1d as a subcircuit. See last 2 pages for the inverter example of this homework.

```
...
X1 1 2 3 4 AND2
...

.subckt AND2 1  2  3  4
... place only CMOS transistors here
.ends
```

Move the CMOS transistors into an AND-gate sub-circuit and refer to this new subcircuit as `"X1 1 2 3 4 AND2"` and place the **.subckt** at the end of the netlist. Re-run the same waveform of 1c. Part 1e should have the same `"plot v(1),v(2),v(3)"` results as part 1d. Hand-in this new netlist containing the subcircuit.

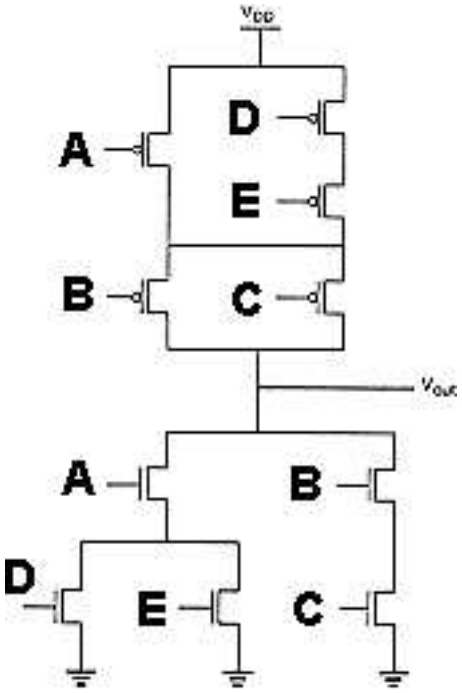
2. Do the following Wakerly problems

(a) 3.80, page 190

(a) 3.39, page 187

3. (a) Given the following CMOS circuit, how many entries (i.e. size of the truth table) for $f(a, b, c, d, e)$? ___

(3b) Determine the boolean expression avoiding the use of a truth table. First, show cases with don't cares (X) and use that for $f(a, b, c, d, e) = V_{out} =$



Hint for Problem 1. Suppose we are doing Figure 3-10 the inverter:

```
*-------------------------------------------
* CMOS Inverter Wakerly, Figure 3-10, page 88
* where Vin is wire 2; Vout is wire 3; Vdd is wire 1; Gnd is wire 0;
* CMOS  Q2=M2=p-channel; Q1=M1=n-channel
*
*Mname DRAIN GATE SOURCE SUBSTRATE MODEL WIDTH   LENGTH
*      NODE  NODE NODE   NODE      NAME  MICRONS MICRONS
*----- ----- ---- ------ --------- ----  ------- ------
M2     3     2    1      1         PCH   W=3.6U  L=1.2U
M1     3     2    0      0         NCH   W=3.6U  L=1.2U
*
*Cname +NODE -NODE VALUE(Picofarads) *** C=CAPACITOR
*----- ----- ----- -----------------
C3     3     0     0.1P
*
*Vname +NODE -NODE VALUE *** V=INDEPENDANT VOLTAGE SOURCE
*----- ----- ----- -----
Vdd    1     0     DC=5.0
*
*Vname +Node -Node Option T1  V1   T2  V2   T3   V3  T4  V4  T5   V5
*----- ----- ----- ------ --  --   --  --   ---- --  --  --  ---- --
Vin     2     0    PWL(   0   0    4N  0    4.1N 3   8N  3   8.1N 0  )
*
*     TSTEP TSTOP
*     ----- -----
.TRAN 0.1N  12N
*
* TEMPERATURE SETTING
*
.OPTIONS TEMP=25 METHOD=GEAR
*
*MODEL NAME TYPE
*----- ---- ----
.MODEL NCH  NMOS (level=2 LD=0.15U TOX=200.0E-10 NSUB=5.37E+15
+ VTO=0.74 KP=8.0E-05 GAMMA=0.54 PHI=0.6 U0=656 UEXP=0.157 UCRIT=31444
+ DELTA=2.34 VMAX=55261 Xj=0.2U LAMBDA=0.037 NFS=1E+12 NEFF=1.001 NSS=1E+11
+ TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 Cj=0.0003 Mj=0.66
+ CJSW=8.0E-10 MJSW=0.24 PB=0.58
.MODEL PCH PMOS (level=2 LD=0.15U TOX=200.0E-10 NSUB=4.33E+15
+ VTO=-0.74 KP=2.70E-05 GAMMA=0.58 PHI=0.6 U0=262 UEXP=0.324 UCRIT=65720
+ DELTA=1.79 VMAX=25694 Xj=0.25U LAMBDA=0.061 NFS=1E+12 NEFF=1.001 NSS=1E+11
+ TPG=1.0 RSH=121.00
+ CGDO=4.3E-10 CGSO=4.3E-10 Cj=0.0005 Mj=0.51
+ CJSW=1.35E-10 MJSW=0.24 PB=0.64
.END
```

And we want to convert this to a .subckt

```
*-----------------------------------------------
* CMOS Inverter Wakerly, Figure 3-10, page 88
*================================================
*X1 A Z Vdd  Z=NOT(A);  *** subcircuit reference ***
X1  2 3 1    NOT2
*================================================
*Cname +NODE -NODE VALUE(Picofarads) *** C=CAPACITOR ***
*----- ----- ----- -----------------
C3     3     0     0.1P
*
*Vname +NODE -NODE VALUE *** V=INDEPENDANT VOLTAGE SOURCE ***
*----- ----- ----- -----
Vdd    1     0     DC=5.0
*
*Vname +Node -Node Option T1  V1   T2  V2   T3   V3  T4  V4  T5   V5
*----- ----- ----- ------ --  --   --  --   ---- --  --  --  ---- --
Vin     2     0    PWL(   0   0    4N  0    4.1N 3   8N  3   8.1N 0  )
*
.TRAN 0.1N  12N
*
.OPTIONS TEMP=25 METHOD=GEAR

*================================================================
* Vin=wire 1; Vout=wire 2; Vdd=wire 3; Observe wires have been re-numbered
.subckt NOT2 1 2 3
*Mname DRAIN GATE SOURCE SUBSTRATE MODEL WIDTH   LENGTH
*      NODE  NODE NODE   NODE      NAME  MICRONS MICRONS
*----- ----- ---- ------ --------- ----  ------- ------
M2     2     1    3      3         PCH   W=3.6U  L=1.2U
M1     2     1    0      0         NCH   W=3.6U  L=1.2U
.ends
*================================================================
.MODEL NCH  NMOS (level=2 LD=0.15U TOX=200.0E-10 NSUB=5.37E+15
+ VTO=0.74 KP=8.0E-05 GAMMA=0.54 PHI=0.6 U0=656 UEXP=0.157 UCRIT=31444
+ DELTA=2.34 VMAX=55261 Xj=0.2U LAMBDA=0.037 NFS=1E+12 NEFF=1.001 NSS=1E+11
+ TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 Cj=0.0003 Mj=0.66
+ CJSW=8.0E-10 MJSW=0.24 PB=0.58
.MODEL PCH PMOS (level=2 LD=0.15U TOX=200.0E-10 NSUB=4.33E+15
+ VTO=-0.74 KP=2.70E-05 GAMMA=0.58 PHI=0.6 U0=262 UEXP=0.324 UCRIT=65720
+ DELTA=1.79 VMAX=25694 Xj=0.25U LAMBDA=0.061 NFS=1E+12 NEFF=1.001 NSS=1E+11
+ TPG=1.0 RSH=121.00
+ CGDO=4.3E-10 CGSO=4.3E-10 Cj=0.0005 Mj=0.51
+ CJSW=1.35E-10 MJSW=0.24 PB=0.64
.END
*-------------------------------------------------------
```