EECS 281: Homework #1 **Due: Tuesday, January 18, 2004**

Name: _____ Email: _____

1. Given the boolean expression: $f(a,b) = (a+b)(\overline{a \cdot b})$

(a) Draw the logic gate schematic:

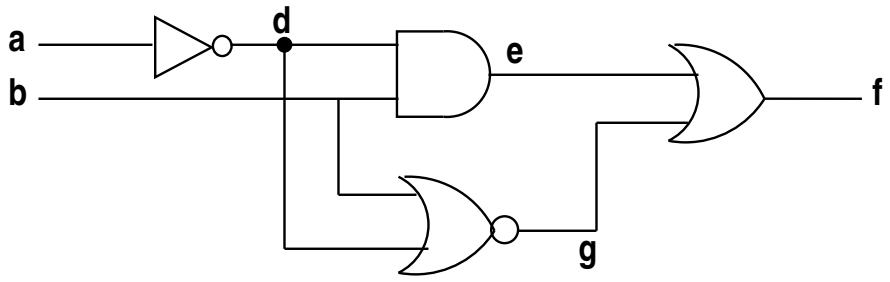
(b) Re-write as a C++/JAVA expression: $f =$ _____

(c) Re-write as a VHDL expression: $f <=$ _____

(d) Fill in the truth table

a b	$a+b$	$a \cdot b$	$\overline{a \cdot b}$	$f = (a+b)(\overline{a \cdot b})$
0 0				
0 1				
1 0				
1 1				

2. Given the following logic circuit



(a) Give the truth table of a, b, c, d, e, g and f:

(b) Give the boolean expression of e, g and f:

e=

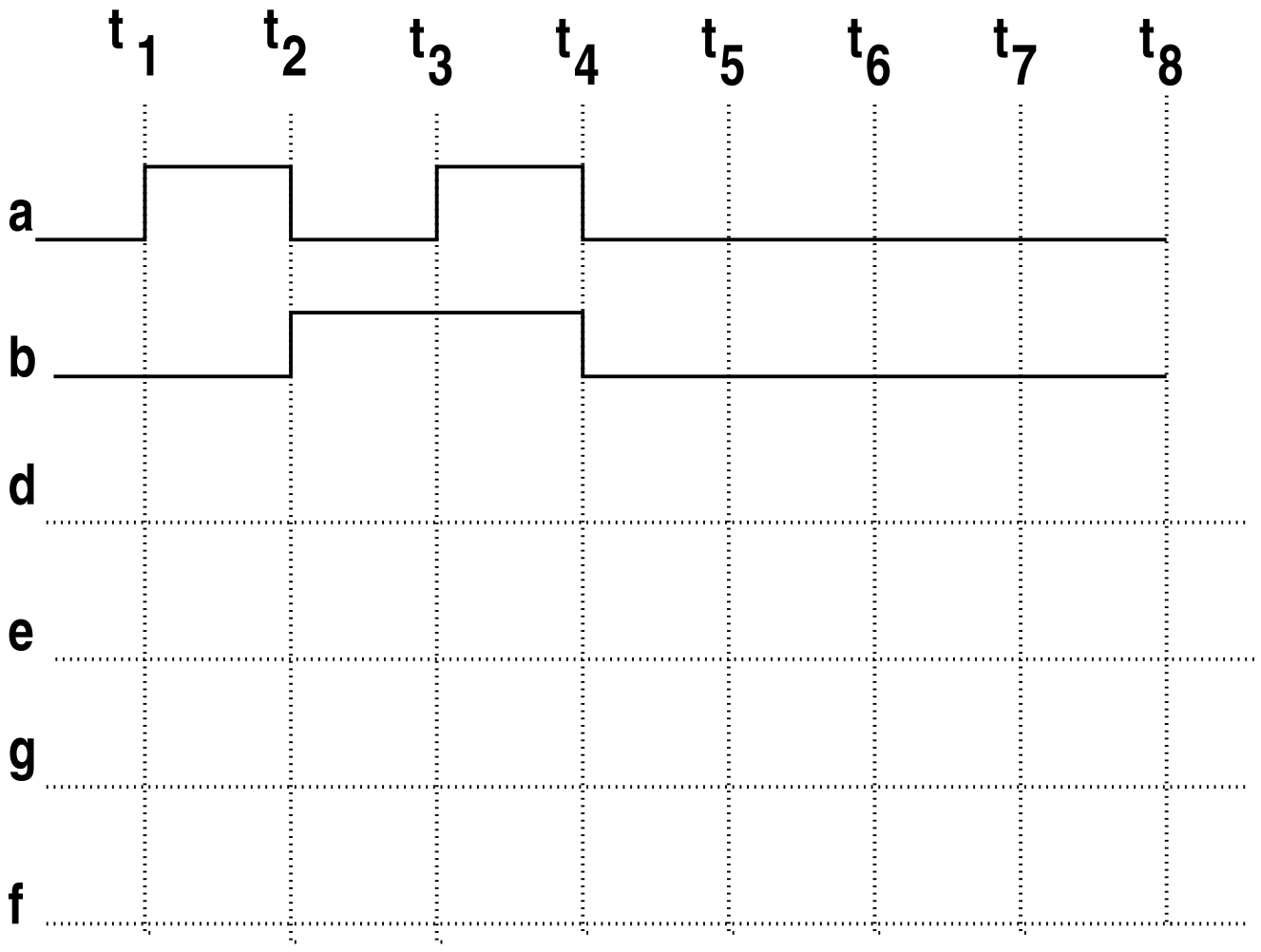
g=

f=

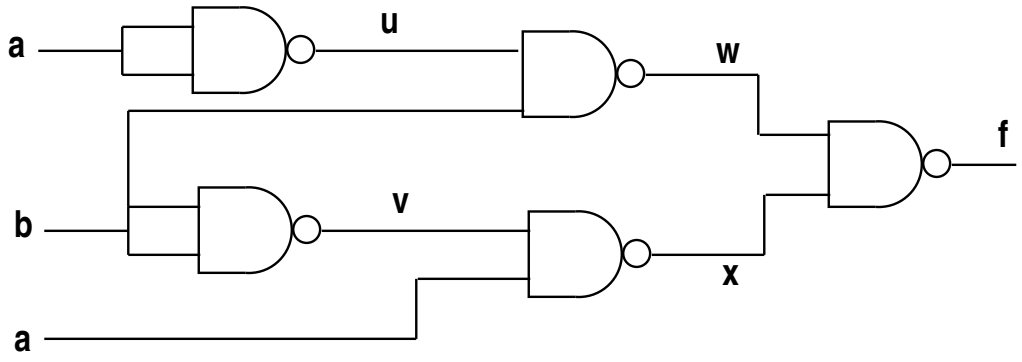
(c) Compare the truth table of part 1d with 2a. Are they the same? Yes or No.

What other common logic function is $f(a, b)$ similar to?

(d) Fill in the timing diagram including trigger lines (0 ns delay) for 2(a).



3. Given the following logic circuit



(a) Give the truth table of a, b, u, v, w, x and f:

(b) Give the boolean expression of $f(a, b) =$ _____

(c) Re-write as a C++/JAVA expression: $f =$ _____

(d) Re-write as a VHDL expression: $f <=$ _____