EECS 281: Extra Credit #2 Due: Thursday, October 21, 2004

Name: _____ Email: _____

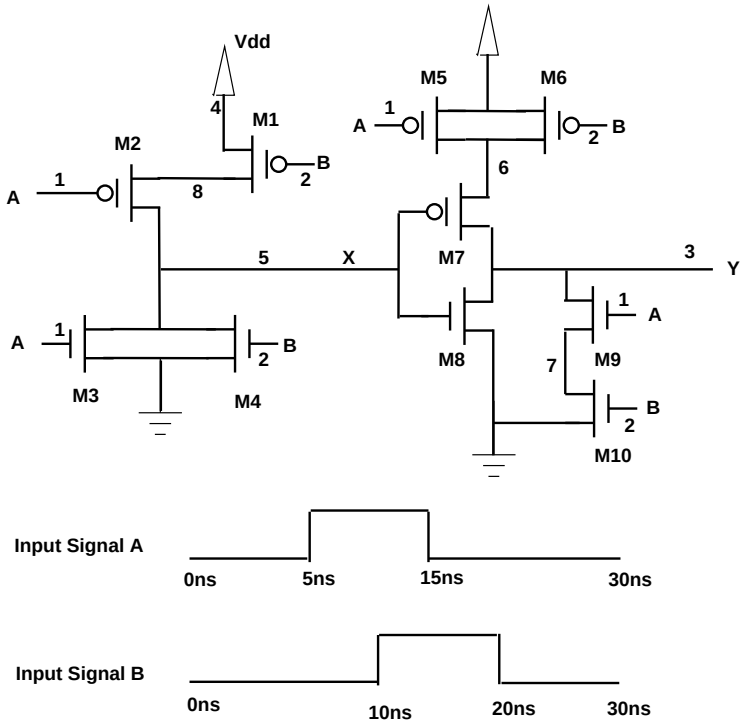

Figure 1: CMOS circuit

x2. (Extra credit 15 points and must complete all parts):
(a) Label all the expected drains (D) and sources (S) in Figure 1.

(b) Fill the truth table for the following CMOS circuit in Figure 1 for nodes.

node 1 (A)	node 2 (B)	node 8	node 5 (X)	node 6	node 7	node 3 (Y)
0	0					
0	1					
1	0					
1	1					

(c) Given the input signals A and B in Figure 1 draw the output signals of X (wire labeled node 5) and Y (wire labeled node 3).

(d) Give the most common behavioral VHDL expression of X<=f(A, B)?

(e) Give the behavioral VHDL expression of of Y<=f(A, B, X)? Is this a OAI or AOI (see Wakerly, page 94)?

(f) Give the most common behavioral VHDL expression of Y<=f(A, B)?

(g) Using (e) and (f), give the complete structural VHDL expression of Y<=f(A, B)?

(g) Draw the structural gate logic schematic for Figure 1.

(h) Download SPICE from "http://www.winspice.com"
and work through the inverter tutorial "http://bear.ces.cwru.edu/eecs_cad/tut_spice3_invertor.html". Then implement Figure 1 in SPICE using the tutorials CMOS models and add a piecewise linear signal for input signals A (node 1) and B (node 2) and Vdd (node 4) of 5 volts. Note: logical 1 is now 5 volts. **Hand-in** the SPICE circuit net-list and input and output voltage and current plots done in part (i). Do not use any capacitors in the circuit and increase the simulation time to 0 to 35 nanoseconds, ".TRAN 0.01N 35N".

(i) Do the following commands: "listing", "run", "display", "plot v(1)", "plot v(2)", "plot v(1),v(2)", "plot v(3)", "plot v(1),v(2),v(3)", "plot v(5)", "plot vdd#branch". If the "plot v(3)" and "plot v(5)" does not match your calculated values for X (node 5) and Y (node 3); most likely you have a wiring error in your spice net-list.

(j) Explain the spikes in the current plot "plot vdd#branch" as to what they mean. Also, why they are not similar in shape as the voltage "plot v(3)".

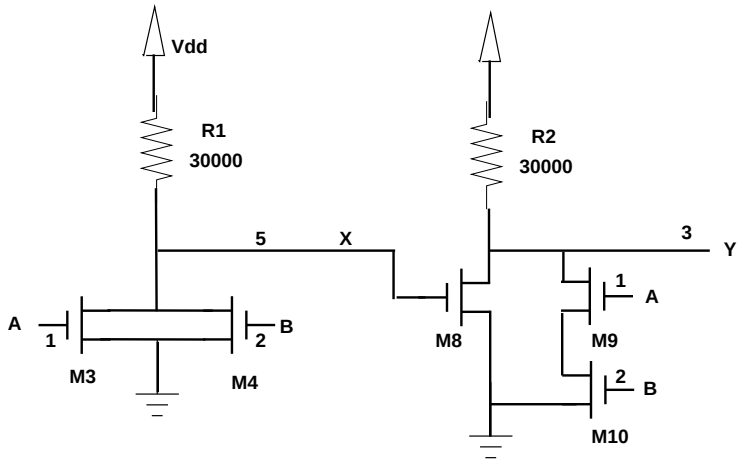

Figure 2: NMOS resistor circuit

(k) Replace the PMOS transistors of Figure 1 with 30000 ohm resistors as shown in Figure 2.
(l) What is the current through the resistor R1 if M3 is on? What is the power of R1?

(m) **Hand-in** and run the same spice simulation steps from part (i) for Figure 2. If the "plot v(3)" is not similar as in part (i), then you have a spice net-list error.

(n) Explain why the current plot of part (i) is different that part (k). Which consumes more power?