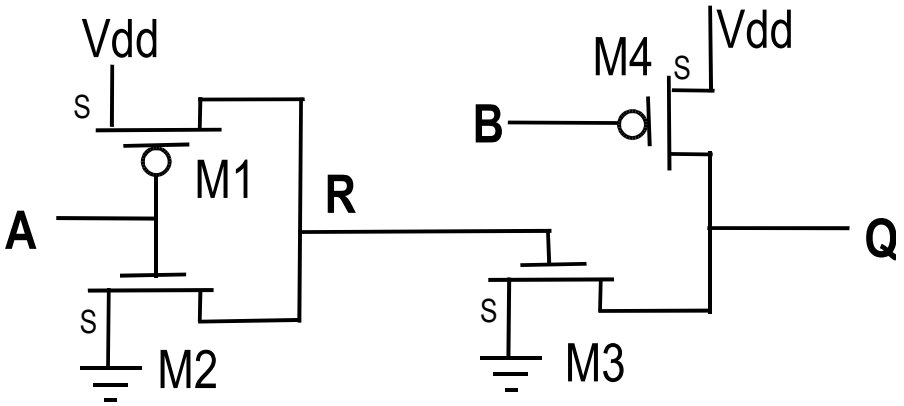
EECS 281 Test 1 (3 pages) Due: Tuesday September 14, 2004

Name: _____ Email:_____ Grade: _____ (100 points max)

(1) (25points) Determine the function table of the following circuit, Vdd=1 Volt (note: possible outputs: 0, 1, X=short, Z=no connection):



Optical illusion: Does everyone see that M1 and M2 form a simple invertor? R=NOT(A)

(Hint: NMOS: if Vg>Vs then ON else OFF; PMOS: if Vg<Vs then ON else OFF.)

Inputs		*M1*				*M2*				*R*	*M3*				*M4*				*Q*
		Vg	*Vs*	*on/off*	*Vd*	*Vg*	*Vs*	*on/off*	*Vd*	*NOT (A)*	*Vg*	*Vs*	*On/ off*	*Vd*	*Vg*	*Vs*	*On/ off*	*Vd*	
A	**B**	**A**	1		**R**	**A**	**0**		**R**		**R**	**0**		**Q**	**B**	**1**		**Q**	
0	0	0	1	on	1	0	0	off	Z	1	1	0	on	0	0	1	on	1	X
0	1	0	1	on	1	0	0	off	Z	1	1	0	on	0	1	1	off	Z	0
1	0	1	1	off	Z	1	0	on	0	0	0	0	off	Z	0	1	on	1	1
1	1	1	1	off	Z	1	0	on	0	0	0	0	off	Z	1	1	off	Z	Z

(8 points) Fill in the following missing SPICE parameters below for the circuit in problem 1.

```
.SUBCKT G1  1 2 3 4
* .SUBCKT G1  A=1 B=2 Q=3 VDD=4 R=5 (Assume)


M1      _5__   _1__  _4__     _4__    _T1__    W=5U    L=2U

M2      _5__   _1__  _0(GND)__0(GND)_X2__    W=5U    L=2U

M3      _3__   _5__  _0(GND)  0(GND)_X2__    W=5U    L=2U

M4      _3__   _2_   __4_       4___    T1__    W=5U    L=2U

.ENDS G1

.MODEL T1 PMOS LEVEL=1 KP=16E-6 LAMBDA=0.044 VTO=-0.85 GAMMA=0.69 PHI=0.7
.MODEL X2 NMOS LEVEL=1 KP=48E-6 LAMBDA=0.032 VTO=0.88 GAMMA=0.66 PHI=0.7
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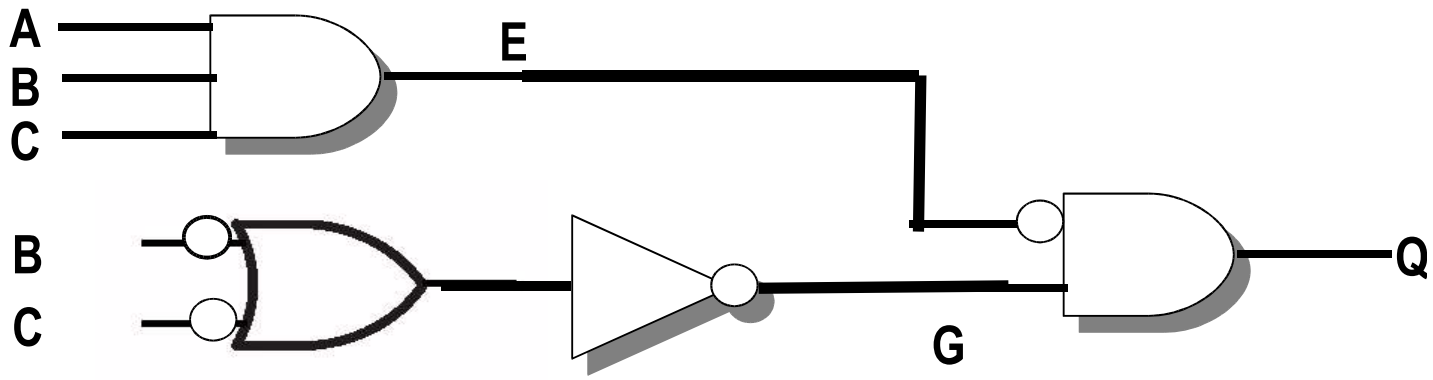
(3) (10 points) Give the logical expression in **VHDL** notation for G and Q in the following logic circuit:



E <= ((A AND B) AND C)

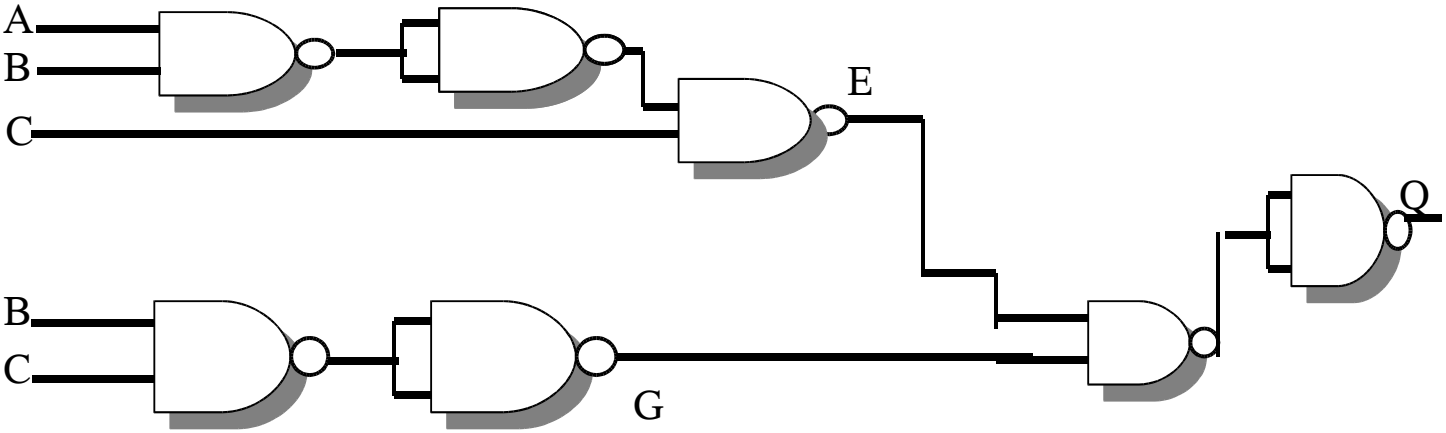
G <= (NOT((NOT(B) OR (NOT(C)))) equivalent simpler expression would be NOT(B NAND C) = B AND C;

Q <=(NOT(A AND B AND C) AND (NOT((NOT(B) OR (NOT(C))))) equivalently could be written as (G AND (NOT(E));

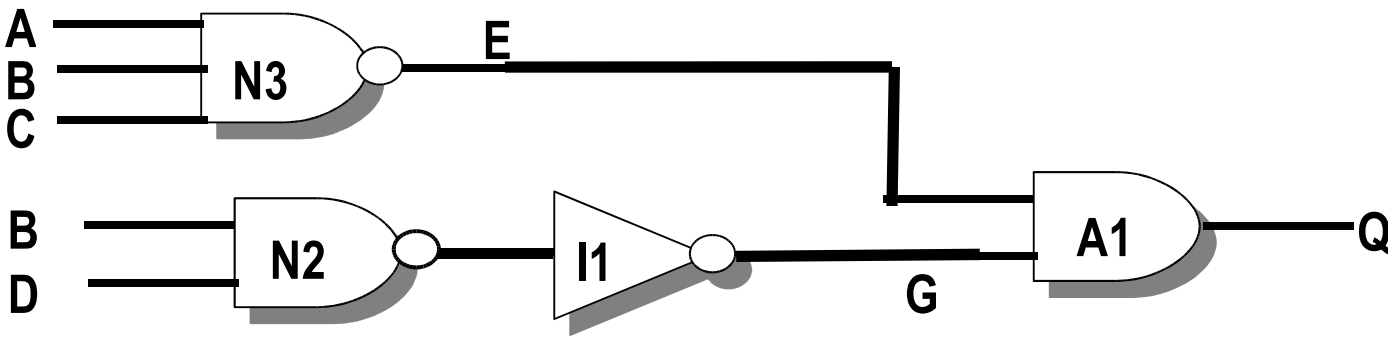
(4) (7 points) Fill in the truth table for problem 3 (note: can use blanks to mean false or zero):

A	*B*	*C*	*E*	*G*	*Q*
0	0	0			
0	0	1			
0	1	0			
0	1	1		1	1
1	0	0			
1	0	1			
1	1	0			
1	1	1	1	1	

(5) (20 points) Redraw problem 3 using only "2-input NAND" gates for output Q only (no 3-input gates allowed):



(6) (15 points) Given that a "NOT" has delay of 10ns, and an "AND" is 20ns for the following circuit what is the maximum delay and show work:



(a) Delay for a 2-input NAND N2 is _____**30ns**_____
(b) Delay for the 3-input NAND N3 is _____**50ns**_____
(c) What is the maximum delay = _____**70ns**_____ and through what gates: **N3,A1 to output Q**_____
and the delay through gates N2, I1, A1 would be 60ns

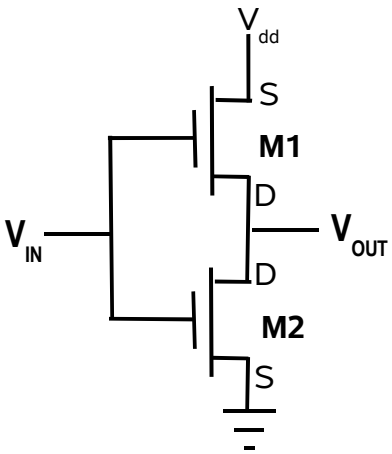
(7) (15 points) Design a **C/C++ logic expression** for a voting machine for a small Ohio town of 3 people (i.e. A, B, C). The voting machine outputs a true if the candidate Q wins the majority of the votes.
Q =((~A & B & C) | (A & C & ~B) | (A & B & ~C) | (A & B & C)); _____

Q is boolean function is often called a majority circuit: Q=Carry=majority(A,B,C); and is the same the carry out of a 1-bit full adder.
1 bit full adder: Sum=odd_parity(A,B,C); Carry=majority(A,B,C);

A	*B*	*C*	*Win?*	*Q*	*ANDs*
0	0	0	No		
0	0	1	No		
0	1	0	No		
0	1	1	Yes	1	~A & B & C
1	0	0	No		
1	0	1	Yes	1	A & C & ~B
1	1	0	Yes	1	A & B & ~C
1	1	1	Yes	1	A & B & C

(X1) (Extra Credit, 5 points): The following circuit contains "only NMOS" transistors what is Vout for a given Vin (Vdd=1 Volt)?
Optical illusion: M1 and M2 form the "lower" part of a 2-input NAND of a CMOS transistor.

The same input Vin is connected to each of the NAND inputs. When Vin=1 then M1 is clearly ON. When M1 is ON the "source of M1" is connected to the "drain of M1" and becomes zero also. Now the "gate of M2" is 1 and the field effect senses the lower voltage on the "labelled" drain and in reality becomes the "real" source. *So, YES, the drain and source are interchangeable according to the voltages on the D and S.* Now, since M2 is ON, then M2 drain at Vout is zero, then M1 is ON since M1 gate is 1 and M1 at Vout is 0, thus M1 is ON. The source of M1 is now connected to drain of M1 which now connects Vdd to ground though M2, leading to a short or X!



Vin	*M1 on/off*	*M2 on/off*	*Vout*
0	Off	Off	Z
1	On	On	X

This is the "only" correct solution using SPICE simulation.

Vin	*M1 on/off*	*M2 on/off*	*Vout*
0	Off	Off	Z
1	Off	On	0

Also accepted answer, if student sticks to the fact M1 source is truly connected to the Vdd.