ECMP 488: *Embedded Systems Design*

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Objective To introduce and expose the student to methodologies for systematic design of embedded systems. The topics include, but are not limited to, system specification, architecture modeling, component partitioning, estimation metrics, hardware software codesign, diagnostics.

Outline

1. Introduction to Embedded Systems. Design methodology and representation. Current CAD design. System-level design.
2. Modeling Techniques. Finite State Machines models. Petri Nets, Event Nets. Data Flow and Control Flow models. Flow Chart-based models. Queueing models.
3. System Architecture Taxonomy. Uniprocessor and Multiprocessor systems. Data path and Control path microarchitecture. Application-Specific architectures. Pipeline architectures. RISC architectures. Superscalar machines. Parallel architectures. Networks.
4. Specification and Representation of Embedded Systems. Behavioral and Structural hierarchy. Data-driven and Control-driven Concurrency. Communication and Synchronization. Timing. Hardware Design languages. VHDL. State Charts.
5. Partitioning Problems of Embedded Systems. Structural Partitioning. Functional and Behavioral Partitioning. Review of Partitioning Algorithms. Resource Allocation of system-level components. Synthesis.
6. Quality Estimation and Design Metrics. Estimation Techniques at the system level. Simulation of system level design. Emulation techniques. System prototyping by programmable logic (FPGAs).
7. Hardware/Software Codesign. Partitioning of Hardware and Software modules. Hardware and Software estimation models. Trade-offs.
8. System-Level Design and Testing. Design for Testability. System level diagnostics. Fault Tolerance techniques.
9. Case Study example. Class Project.

General References

1. W. Wolf, "Hardware-Software Co-Design of Embedded Systems, *Proc. IEEE*, V. 82, No. 7, July 1994.

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3. A. Kalavade, E. Lee, "A Hardware-Software Methodology for DSP Applications," *IEEE Design and Test*, V. 10, No. 3, 1994.

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1 References Concerning Partitioning

1. E. D. Lagnese, D. Thomas, "Architectural Partitioning of System Level Synthesis," *IEEE Trans. on CAD*, V. 10, No. 7, JUly 1991.

2. F. Vahid, D. Gajski, "Specification Partitioning for System Design," *Design Automation Conf.*, 1992.

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6. B. Kernigham, S. Lin, "An efficient heuristic procedure for partitioning graphs," *Bell System Technical Journal*, Feb. 1970.

2 References Concerning Modeling

1. W. Reisig, *A Primer in Petri Nets*, Springer Verlag, New York, 1992.

2. D. Harel, "Statecharts: A Visual Formalism for Complex Systems," *Science of Computer Programming*, 8, 1987.

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   F. Hady, J. Aylor, R. Williams, R. Waxman, "Uninterpreted modeling using VHDL," *Internat. Conf. on Computer-Aided Design (ICCAD-88)*, 1988.

4. F. Vahid, S. Narayan, D. Gajski, "SpecCharts: A Language for System Level Synthesis," *Internat. Symp. on Computer Hardware Description Languages and their Applications,* 1991.

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3 Other References

1. D. Lanneer, S. Note, F. Depuydt, M. Pauwels, F. Catthoor, G. Goosens, H. De Man, "Architectural Synthesis for Medium and High Throughput Signal Processing with the new CATHEDRAL Environment," In R. Compasano and W. Wolf, Editors, *High Level VLSI Synthesis*, Kluwer Academic Publishers, Boston, 1991.

2. J. Gong, D. Gajski, S. Narayan, "Software Estimation from Executable Specifications," *Journal of Computer and Software Engineering*, 1994.

3. W. Ye, R. Ernst, T. Benner, J. Henkel, "Fast timing analysis for hardware-software co-synthesis," *Internat. Conf. Computer Design (ICCD-93)*, 1993.

4. M. Srivastava, T. Blumenau, R. Brodersen, "Design and Implementation of a robot control system using a unified hardware-software rapid prototyping framework," *Internat. Conf. Computer Design (ICCD-92)*, 1992.

   P. Paulin, C. Liem, T. May, S. Sutarwala, "DSP design tool requirements for embedded systems," *J. VLSI Signal Processing*, 1994.